24LCS21

1K 2.5V Dual Mode I²C™ Serial EEPROM

FEATURES

- Completely implements DDC1™/DDC2™ interface for monitor identification
- Hardware write-protect pin
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible (SCL)
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 100 kHz (2.5V) and 400 kHz (5V) compatibility (SCL)
- 10,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I) -40°C to +85°C

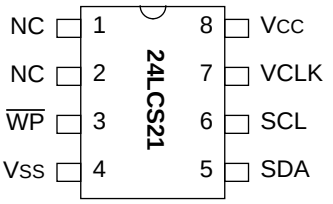
DESCRIPTION

The Microchip Technology Inc. 24LCS21 is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit Only Mode and bi-directional Mode. Upon power-up, the device will be in the Transmit Only Mode, sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the bi-directional Mode, with byte selectable read/write capability of the memory array in standard I²C protocol.

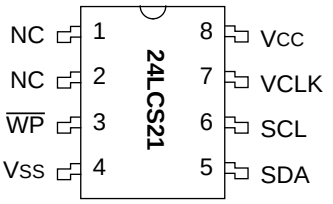
The 24LCS21 also enables the user to write-protect the entire memory contents using its write-protect pin. The 24LCS21 is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPES

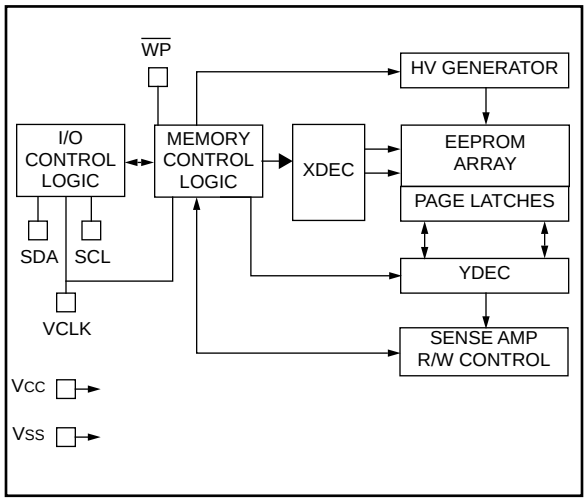
PDIP



SOIC



BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{WP}$	Write Protect (active low)
V_{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
V_{CC}	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

	V_{CC} = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	V_{IH}	0.7 V_{CC}		V	
Low level input voltage	V_{IL}		0.3 V_{CC}	V	
Input levels on VCLK pin:					
High level input voltage	V_{IH}	2.0	0.8	V	$V_{CC} \geq$ 2.7V (Note)
Low level input voltage	V_{IL}		0.2 V_{CC}	V	V_{CC} < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	V_{HYS}	.05 V_{CC}	—	V	(Note)
Low level output voltage	V_{OL1}		0.4	V	I_{OL} = 3 mA, V_{CC} = 2.5V (Note 1)
Low level output voltage	V_{OL2}		0.6	V	I_{OL} = 6 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = 0.1V to V_{CC}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = 0.1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{INT}		10	pF	V_{CC} = 5.0V (Note1), Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} Write	—	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
	I_{CC} Read	—	1	mA	
Standby current	I_{CCS}	—	30	µA	V_{CC} = 3.0V, SDA = SCL = V_{CC}
			100	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC}

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc= 2.5-5.5V		Vcc= 4.5 - 5.5V		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	100	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	10M	—	10M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

2.0 FUNCTIONAL DESCRIPTION

The 24LCS21 operates in two modes, the Transmit-Only Mode and the bi-directional Mode. There is a separate two wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bi-directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional two wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00H) and continue. The bi-directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After VCC has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT ONLY MODE

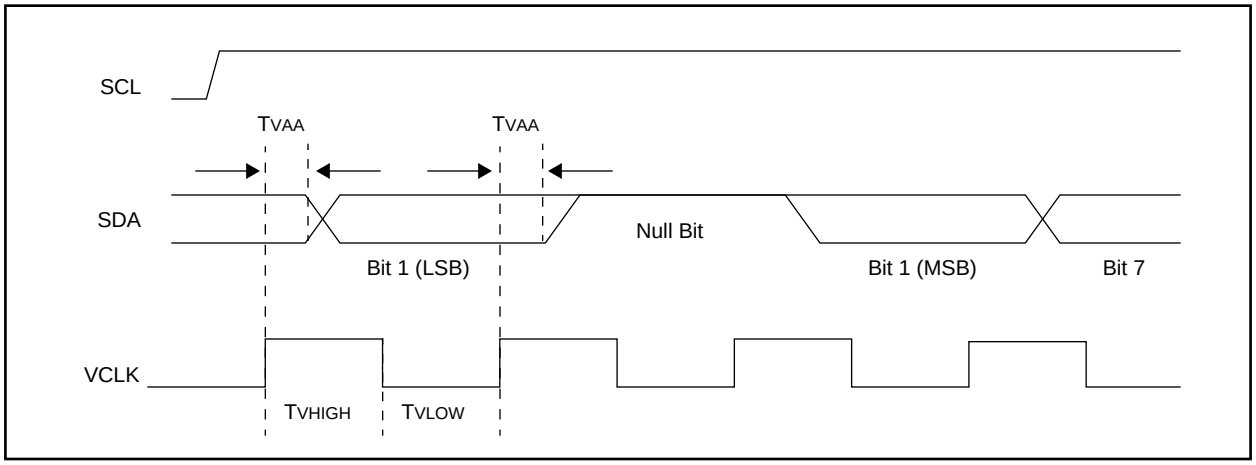
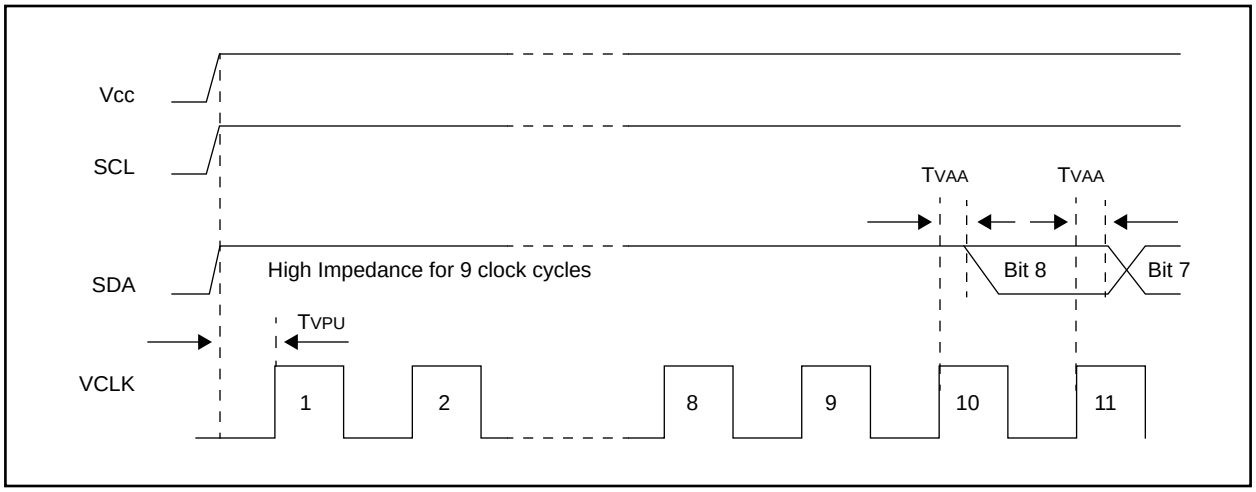


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

The 24LCS21 can be switched into the bi-directional Mode (Figure 3-1) by applying a valid high to low transition on the bi-directional Mode Clock (SCL). When the device has been switched into the bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire bi-directional data transmission protocol (I^2C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LCS21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

In this mode, the 24LCS21 only responds to commands for device 1010 000X.

3.1 Bi-directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-2).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

FIGURE 3-1: MODE TRANSITION

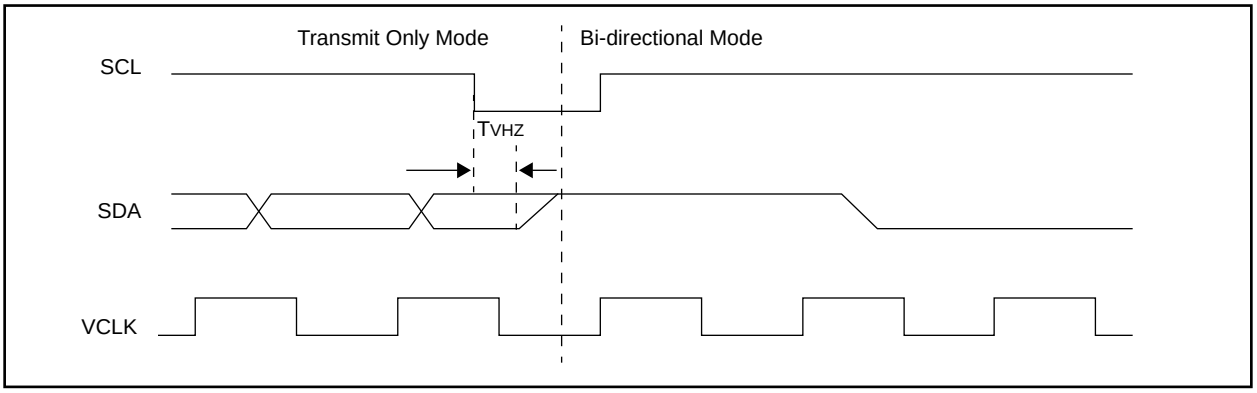
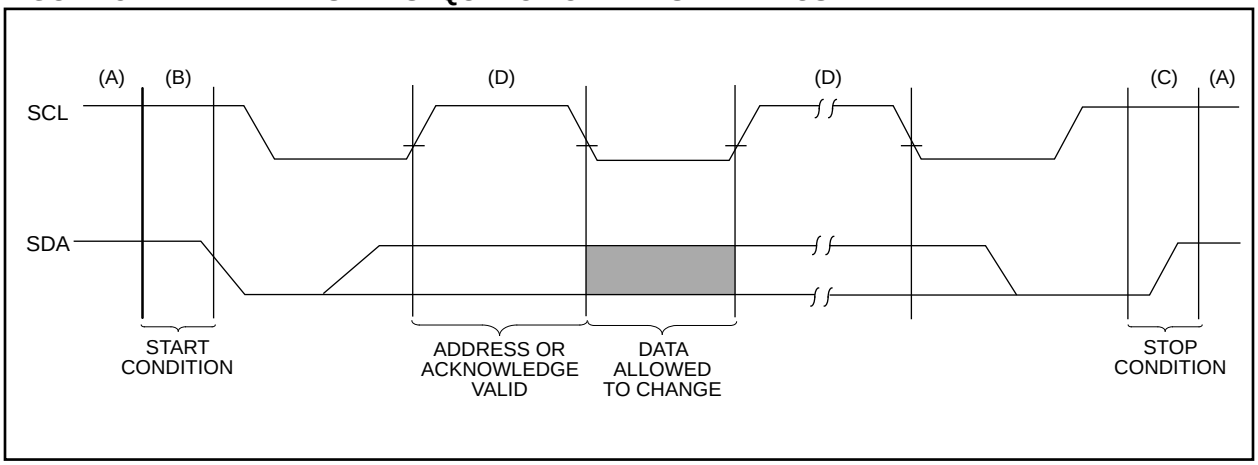


FIGURE 3-2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Note:	Once switched into bi-directional Mode, the 24LCS21 will remain in that mode until power goes away. Removing power is the only way to reset the 24LCS21 into the Transmit-only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LCS21 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-3: BUS TIMING START/STOP

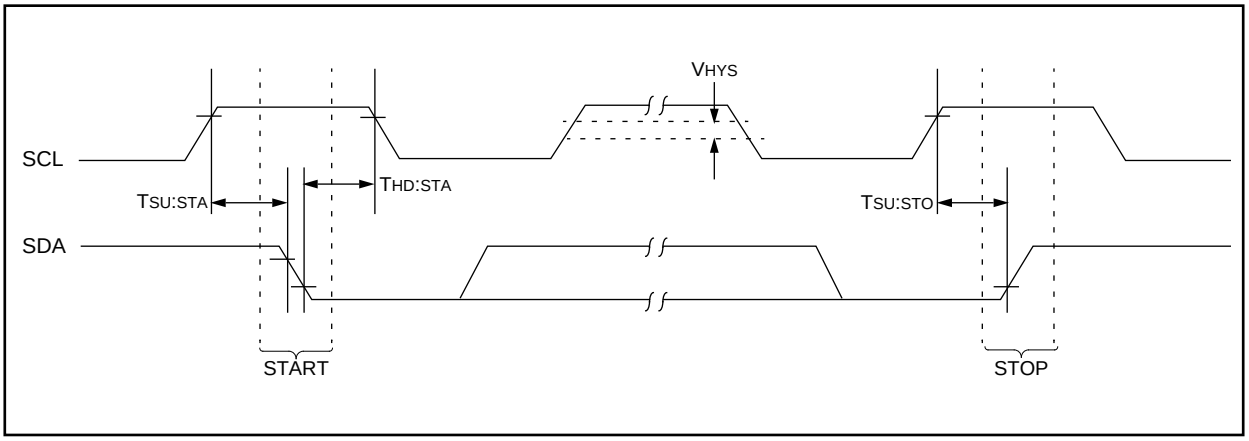
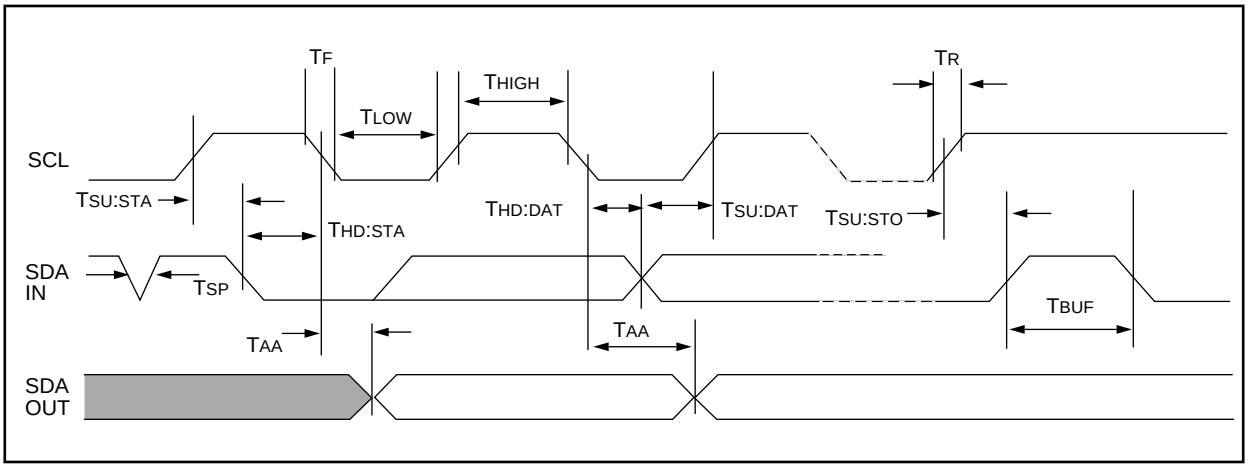


FIGURE 3-4: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

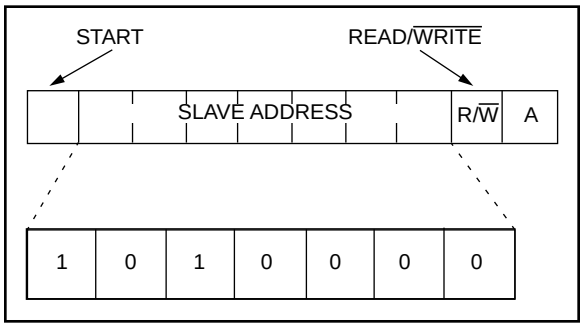
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LCS21.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LCS21 (Figure 3-5).

The 24LCS21 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-5: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (4 bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LCS21. After receiving another acknowledge signal from the 24LCS21 the master device will transmit the data word to be written into the addressed memory location. The 24LCS21 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS21 will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

FIGURE 4-1: BYTE WRITE

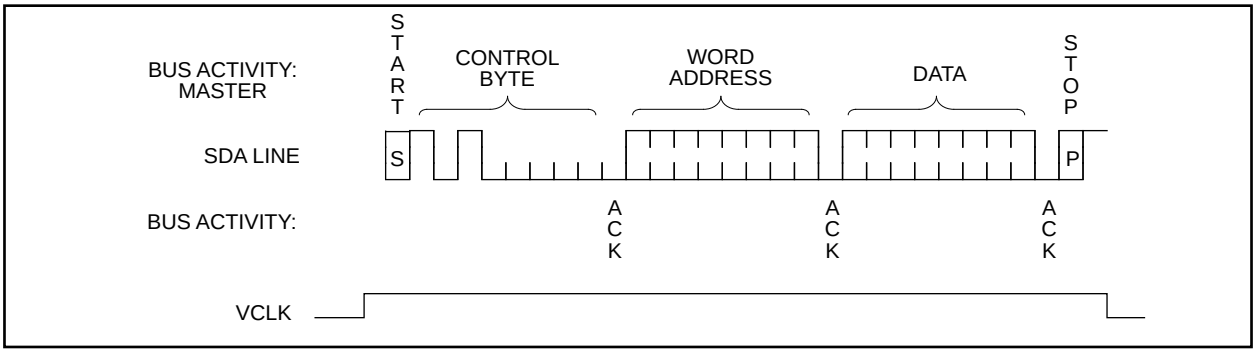
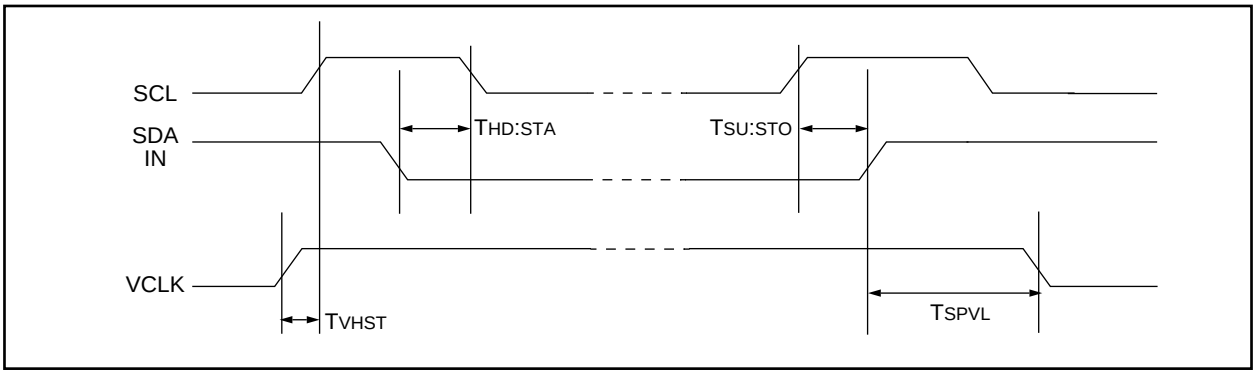


FIGURE 4-2: VCLK WRITE ENABLE TIMING



4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LCS21 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LCS21 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW

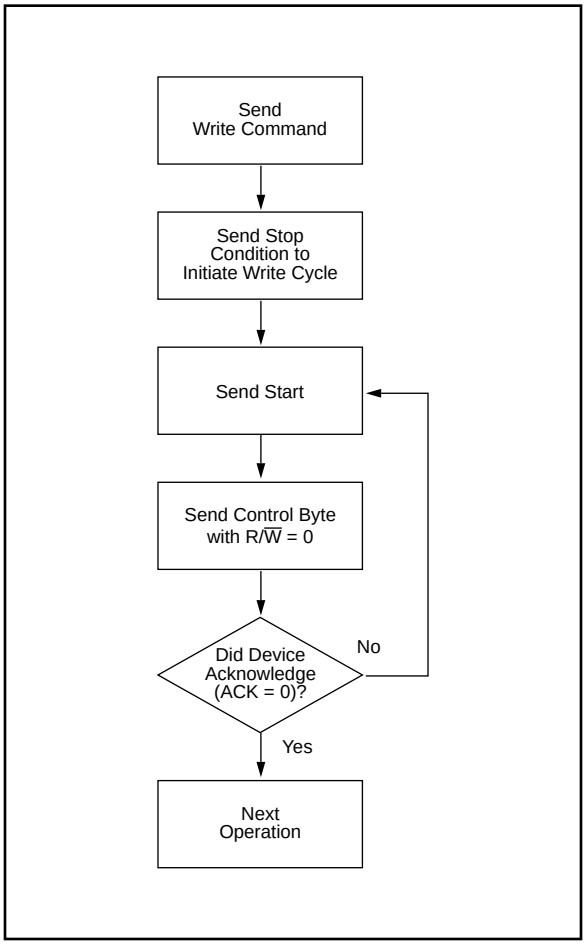
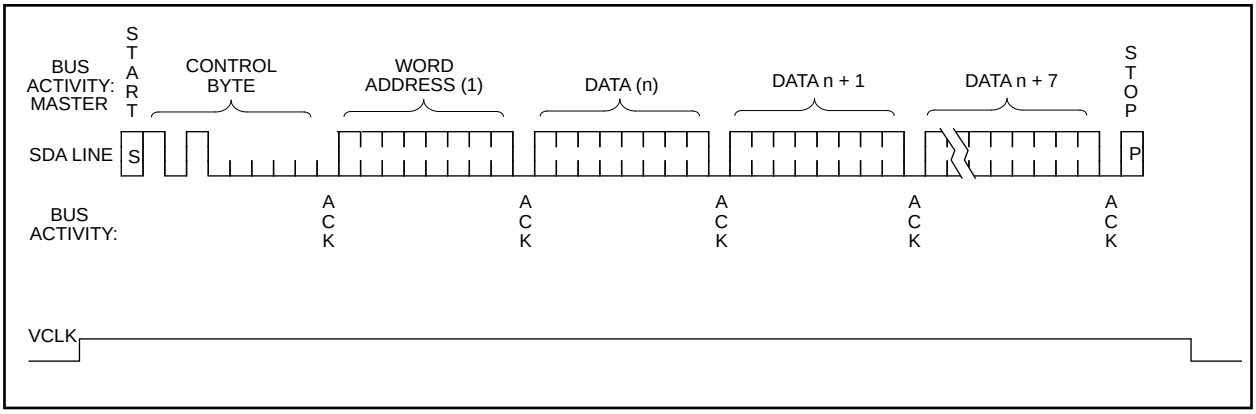


FIGURE 5-2: PAGE WRITE



6.0 WRITE PROTECTION

When using the 24LCS21 in the bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the 24LCS21 to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, Pin 3 performs a flexible write protect function. The 24LCS21 contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the $\overline{WP}$ pin. Until this fuse is set, the 24LCS21 is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS21 is determined by $\overline{WP}$ (Figure 6-1).

FIGURE 6-1: WRITE PROTECT TRUTH TABLE

VCLK	$\overline{WP}$	Add. 7Fh Written	Mode
0	X	X	Read Only
1	X	No	R/$\overline{W}$
1	1/open	Yes	R/$\overline{W}$
1	0	Yes	Read Only

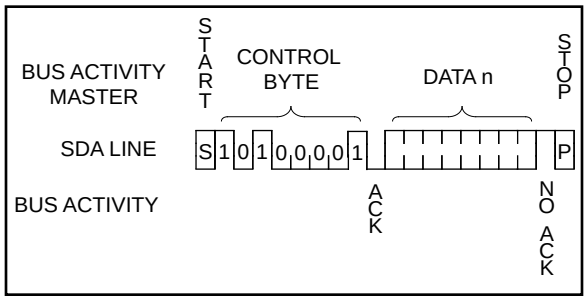
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LCS21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LCS21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21 discontinues transmission (Figure 7-1).

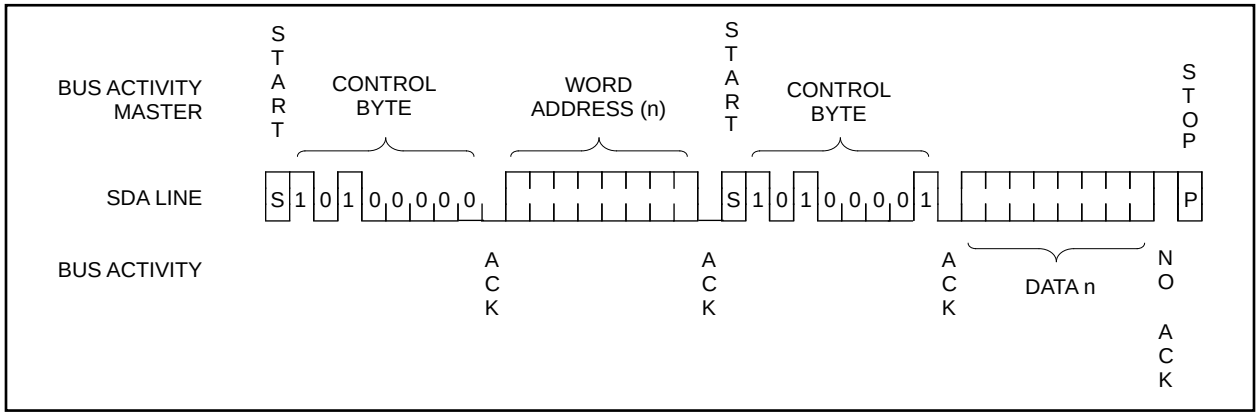
FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS21 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LCS21 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21 discontinues transmission (Figure 7-2).

FIGURE 7-2: RANDOM READ



7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS21 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS21 to transmit the next sequentially addressed 8-bit word (Figure 8-1).

To provide sequential reads the 24LCS21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LCS21 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10 KΩ for 100 kHz, 1 KΩ for 400 kHz).

For normal data transfer in the bi-directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL

This pin is the clock input for the bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit Only Mode to the bi-directional Mode. It must remain high for the chip to continue operation in the Transmit Only Mode.

8.3 VCLK

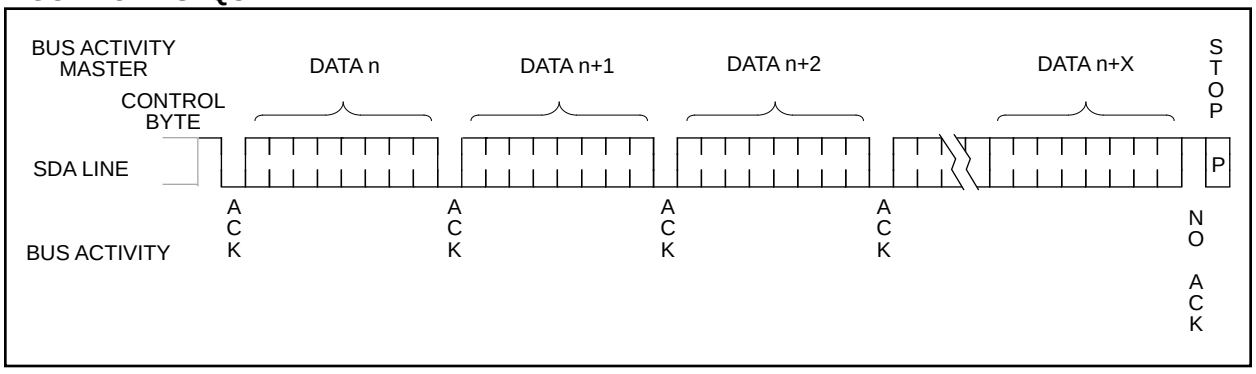
This pin is the clock input for the Transmit Only Mode (DDC1). In the Transmit Only Mode, each bit is clocked out on the rising edge of this signal. In the bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 $\overline{WP}$

This pin is used for flexible write protection of the 24LCS21. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the 24LCS21 (Figure 6-1).

The $\overline{WP}$ pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1) at all times if this pin is floated.

FIGURE 8-1: SEQUENTIAL READ



24LCS21 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

24LCS21 – __ /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank	=	0˚C to +70˚C
	I	=	-40˚C to +85˚C
Device:	24LCS21		Dual Mode I^2C Serial EEPROM
	24LCS21T		Dual Mode I^2C Serial EEPROM (Tape and Reel)

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972 991-7177 Fax: 972 991-8588

Dayton
Microchip Technology Inc.
Suite 150
Two Prestige Place
Miamisburg, OH 45342
Tel: 513 291-1654 Fax: 513 291-9175

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technmgy Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905 405-6279 Fax: 905 405-6253

ASIA/PACIFIC

China
Microchip Technology
Unit 406 of Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hongiao District
Shanghai, Peoples Republic of China
Tel: 86 21 6275 5700
Fax: 011 86 21 6275 5060

Hong Kong
Microchip Technology
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

India
Microchip Technology
No. 6, Legacy, Convent Road
Bangalore 560 025 India
Tel: 91 80 526 3148 Fax: 91 80 559 9840

Korea
Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore
Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan, R.O.C
Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 1628 850303 Fax: 44 1628 850178

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleone Pas Taurus 1
Viale Colleoni 1
20041 Agrate Brianza
Milan Italy
Tel: 39 39 6899939 Fax: 39 39 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

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